University of Southern California ISI-West
4676 Admiralty Way, Suite 1001, Marina del Rey, CA 90902-6695

Innovative Prototyping Systems (DMOSFAB)

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Inclusive of Delivery Orders 0001, 0002 and 0003

FINAL TECHNICAL REPORT

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Submitted by

University of Southern California
Information Sciences Institute
Silicon Systems Division

Technical Point of Contact	Administrative Point of Contact
César Piña, cpina@MOSIS.ORG	Beverly Hartmeyer, beverlyh@isi.edu
Tel: (310) 448-9195 FAX: (310) 823-5624 4676 Admiralty Way Suite 1001 Marina del Rey, CA 90292-6695	Tel: (310) 822-1511 FAX: (310) 822-1869 4676 Admiralty Way Suite 1001 Marina del Rey, CA 90292-6695

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I. TASK OBJECTIVE:

The objective of this program was to provide cost effective rapid access to state of the art U.S. Microelectronics Industry fabrication technology for DoD customers and the NSF educational community. Establishing a prototyping service for use provided this access to the DARPA and NSF research communities offering multiple technologies not obtained from a single fabrication vendor. This service satisfied the goals of the Defense Advanced Research Projects Agency by providing state-of-the-art VLSI fabrication services and electronic systems assembly technology and ensuring that the country's newly emerging engineers would be able to support military needs in the area of electronics.

II. TECHNICAL PROBLEMS

1.0 COSTS

One of the main problems facing a researcher who needs to access state of the art IC fabrication technology, is the high cost of individual (dedicated) fabrication runs. Using a multiproject service with "shared" fabrication runs, however, reduces this cost significantly. To a first order approximation, the cost of an individual project is then equal to the cost of the fabrication run divided by the number of users in the run. These fabrication costs are technology dependent: feature sizes smaller than 2_μ, require the use of stepper based technology to obtain a reasonable yield. During the course of this work, the majority of the wafer fabricators using stepper based technology, employed reticles with dimensions ranging from 12mm to 20mm, with feature sizes five times (5X) the size of the printed feature on the wafer. For example, a 1_μ feature appears on the reticle as 5_μ. The reticle is then stepped across the wafer 25 or more times, compared to once for full wafer lithography. This eliminates the yield problems associated with aligning a 1_μ feature across a 150mm wafer, but it reduces the payload available for prototyping from 6000 sqmm in full wafer lithography, to some area between 200 and 400 sqmm. If we assume that the cost of a typical fabrication run is of the order of $75k, and that the users all submit projects of the same size, then the user's cost is as shown in the following table:

TECHNOLOGY	NUMBER OF USERS	COST/PROJECT
2.0_μ (FWL)	150	$ 500
1.2_μ (1X)	35	$ 2,150
0.8_μ (5X)	15	$ 5,000

NOTE: FWL means Full Wafer Lithography.
1X means 1X Stepper Lithography
5X means 5X Stepper Lithography

The type of lithography employed determines the number of users per fabrication run, which is in turn governed by the technology accessed. To be more specific, the minimum feature size is the controlling factor. The smaller the feature sizes the higher the cost. This makes 5X-stepper technology more expensive than FWL 2_μ technology, because the reduced payload area limits the number of users to 15 per run. In an attempt to reduce these costs, other approaches were investigated. For example, if reticle management systems were used, the cost per project for the 0.8um size could be further reduced to $2,500 or perhaps $1,000 each. Another approach considered was the use of direct write on wafer (DWW) processes. Significant technical and economic problems, however, existed for both of these approaches, and no viable solution was obtained.

Vendor selection for any given technology was based on performance, yield, and availability at the time of initial selection. An additional factor in selecting IC fabricators is that the volume of business from a given customer needs to have a certain "critical mass" to be attractive to a particular fabricator. This critical mass or volume is very dependent upon existing economic conditions as well as the type of business sought by

the IC fabricator, but in any case, limits the number of fabricators the broker can use for a given technology.

2.0 TECHNOLOGY ACCESS and VENDOR INTERFACES

The individual researcher, even if adequate funding is available, is then faced with the simple problem of whether the fabricator will even deal with someone having very low volume requirements. The broker's business, on the other hand, becomes attractive to the wafer fabricator because of the large number of designs processed by the broker, and hence larger volume of business for the fabricator.

Another problem that faces the researcher, is the task of establishing vendor interfaces, to one or to a set of vendors. For a large number of users it becomes a matter of significant effort duplication by each of the research individuals. Assuming, of course, that adequate funding was available to support a large number of dedicated fabrication runs, and that the IC fabricators are willing to deal with a multitude of users requiring only a small number of parts. This process can be likened to reinventing the wheel for each individual case. The interfaces required, are extensive, from correction factors ("bloat and shrink" factors) applied to the as-drawn design geometry to insure that the designer receives designs with the feature sizes he/she specified to the layers used for the different processes and the field polarity required for the phototooling. In contrast to individual designer/fabricator interfaces, the broker does this once for each fabricator and/or technology and the details are then transparent to the designer, who is free to concentrate on the details of his own research rather than on the manufacturing details.

III. TECHNICAL RESULTS

1.0 PRIMARY FUNCTION

The primary function of the MOSIS IC Brokerage Service established by USC/ISI to meet the requirement of this contract was to provide access to cost effective, advanced technology fabrication for the research and educational communities. A set of *basic principles* was formulated in conjunction with the Defense Advanced Research Projects Agency during the subject contract to guide the operation of the Service. These are stated below.

2.0 BASIC PRINCIPLES OF MOSIS OPERATIONS

(1) Service research and educational institutions (MOSIS' primary customers).

Tiny Chips for NSF/DARPA Educational uses.
PCB Service
Technology Files for Design Tools
Technologies for Advanced Designs
Project Management

(2) Serve as Neutral Third Party between Designer and Fabricator

Independent yield and performance monitor
Provide stable monitoring of foundries to assist designers

(3) Provide consistent and uniform access to multiple technologies

Provide continuous introduction of new technology and services

Available Technologies during the contract duration:

Digital CMOS: 2μ, 1.2μ, 0.8μ, 0.5μ, 0.35μ, 0.25μ
Analog CMOS: 2μ and 1.5μ
PCB's;
GaAs;
MCMs (MultiChip Modules);

Expected Future Technologies:
Digital CMOS with Analog options: 0.18, 0.15 μ
5V/12V Analog CMOS:
MEMS;

(4) Lower Prototyping Costs Through Multi-Project Concept

Cost to user ~ Cost of run/Number of users
Full-wafer lithography for 2um feature sizes = 80-200 users/run.
1X Stepper lithography for 1.2μ feature sizes = 10-30 users/run
5X Stepper lithography for 1.2-0.5μ feature sizes = 5-20 users/run

(5) Ensure High and Uniform Product Quality

Product quality monitored independently of the wafer fabricator's tests.
Parametric test structures, yield monitor circuits and statistical control charts
Defect density statistics maintained on all vendors.

(6) Provide Vendor Independence in Multiple Technologies

Possible through the use of generic, scaleable design rules

MOSIS TECHNOLOGIES AND FABRICATORS DURING THE PERFORMANCE OF THE CONTRACT

TECHNOLOGY	***VENDORS***
2.0μ CMOS (Analog options)	*Orbit*
0.5-1.5μCMOS/BiCMOS (Analog options)	*AMI*
1.2μCMOS	*HP NID*
0.8μ CMOS	*HP NID*
0.5 μ CMOS	*HP NID*
0.35 μ CMOS	*TSMC*
0.25 μ CMOS	*TSMC*
1.0μ GaAs	*Vitesse*

(7) Introduce Experimental Technologies Rapidly and Economically

The marginal cost incurred by MOSIS in introducing GaAs technology was approximately $95K.

3.0 GENERAL METHODOLOGY

Designers submitted their designs using either electronic mail or magnetic media to the MOSIS Service of USC/ISI. The MOSIS Service collected and merged the separate designs into a single phototooling set. The projects were then included in regularly scheduled fabrication runs through U.S. commercial phototooling, wafer fabricators and device assembly houses. The Service provided U.S. researchers with access to multiple fabricators and multiple advanced technologies, while maintaining low prototype costs. The latter is accomplished through the use of shared project fabrication runs. To minimize the access problem USC/ISI developed simple sets of forms that contained a uniform set of requirements for the different classes of users, such as DARPA Research, University classes, DoD contractors, etc.

4.0 OPERATION OF THE MOSIS IC PROTOTYPING SERVICE

4.1 INTRODUCTION

The Information Sciences Institute of the University of Southern California operated the MOSIS silicon prototyping service for the duration of this contract. The MOSIS service provided fast turnaround fabrication of integrated circuits in prototype or small production quantities to over 100 DARPA and NSF sponsored organizations. A moderate number of DoD contractors also made use of the prototyping service for their research efforts. The MOSIS service subcontracted for IC fabrication with commercial firms and provided designers an interface to the semiconductor industry. Users submitted designs to MOSIS using either electronic mail or magnetic tapes and received packaged parts in a few weeks. Accessing the US semiconductor industry through the MOSIS service drastically reduced the risk, time, and cost of system development based on custom and semi-custom chips. MOSIS provided a single and relatively constant interface to an industry known for its multitude of different interfaces and rapid technological changes. The following sections will discuss the management of the functions performed by the MOSIS Service.

4.2 ORGANIZATIONAL STRUCTURE

The Information Sciences Institute is divided into separate Divisions, each of which is subdivided into separate Projects. The individual Divisions are responsible for the technical performance of specific contractual tasks, while functions such as accounting, procurement, legal functions, computer operations, etc. are provided to the operating divisions by the Institute and/or the University. The costs for each of these functions are shared by the divisions and are categorized under the heading of Common and O&M costs. The MOSIS Service is a Project within the Silicon Systems Division.

4.3 PROTOTYPING SERVICE ACCESS

Access to IC chip fabrication was provided through multiproject fabrication runs where designs from the research community were submitted in tape or via electronic mail, merged together at USC/ISI, and then fabricated through commercial fabrication houses. An accounting system was maintained to provide detailed information on the nature, composition and costs of the fabrication runs.

4.4 MOSIS OPERATIONS

The MOSIS Service managed the data and logistics needed to allow designers to design and then convert their geometrical data into packaged parts. It utilized the commercial semiconductor industry for all manufacturing steps.

Geometrical and design data from different designers was assembled into phototooling (mask) data specifically targeted towards various wafer fabricators. The designer's geometrical description of the chip being fabricated was accepted in one of several commonly used descriptive formats such as CALMA GDSII, MEBES, and CIF. Each fabrication line received masks exactly the way their own masks are prepared, and with the precise geometry needed to process wafers. This geometry typically consists of alignment marks, critical dimension marks, and the fabricator's process control monitors, allowing the fabricator to determine whether the process specifications have been met. The transformations of the designer's geometry are completely transparent to the device designer, who is then free to concentrate on the design itself, rather than on the mechanics of mask procurement. The merging together of a number of different designs on one mask set had the additional advantage of sharing the cost of fabrication among a number of users, the individual cost of the project being then a fraction of the total cost of a dedicated manufacturing run. Mask fabrication was obtained through commercial vendors having E-beam mask making equipment. The mask manufacturers were provided with tapes containing the pattern files and a control file known as a job deck that specified the location on each mask where the pattern file has to be written. The mask manufacturers simply loaded the tapes and turned on the equipment that was then completely controlled by the MOSIS written tapes.

Wafer fabrication was also obtained from commercial semiconductor manufacturers. Stability of manufacturing lines and processes as well as volume capacity for those products requiring volume production were the principal reasons for the selection by MOSIS of vendors to the commercial sector. Among the vendors used and/or evaluated were: Hewlett Packard, VLSI Technology Inc., Orbit Semiconductor Corp., Gould AMI, Vitesse Semiconductor Corp., IBM, TSMC, National, Motorola, and UTMC. The wafers were purchased on the basis of the fabricator's wafer process specifications, no special "tweaking" of the manufacturing processing was required from the manufacturer. The manufacturer's process specifications form the basis for the acceptance of the wafers both at the semiconductor fabricator and later, at the MOSIS test facility.

4.5 VENDOR SELECTION

Vendors were selected on the basis of competitive bids, final selection was done only after evaluation test runs are completed. Requests for quotations were sent to fabricators that were initially selected on the basis of their technological capability in the areas of interest. These requests contained non-disclosure agreements, MOSIS wafer acceptance specifications, MOSIS geometrical design rules, etc. Upon receiving a vendor response of interest, the process of qualification begins. The vendor's geometrical descriptions of their test structures, critical dimension figures, alignment marks, etc. were first obtained and these were then incorporated into the run-closing software. The next step involved the generation of test masks, incorporating both the wafer vendor's structures as well as the necessary MOSIS structures. Once both MOSIS and the wafer fabricator approved these test masks, a preliminary evaluation run was prepared containing an extensive number of test structures as well as some functional circuits of known behavior. Approval for regularly scheduled runs was given once the structures on the test run are successfully evaluated and DARPA's concurrence obtained.

4.6 FABRICATION RUN CONTROL

Submitted design layout files of projects were screened by an automated check for valid syntax prior to being placed in the fabrication queue. Checks were made also for valid technology parameters, validity of account being charged, etc. before the project was assigned to a fabrication run. At the time a run is closed, all the information pertaining to the run was placed in a "RUN BOOK." This book is used by all the personnel involved in the processing of the particular run, and contains all the information generated during run processing. The information contained in the run book includes applicable work orders, mask inspection data, project bonding diagrams, wafer test data, etc. and serves as a complete history of the run. An operational manual describes the run closing process in detail.

4.7 PRODUCT ACCEPTANCE

Wafers received by MOSIS contained the manufacturer's process control monitors, as well as a set of MOSIS developed parametric test structures and yield monitors to measure the defect density of a particular run. Final acceptance of the finished wafers occurs at the MOSIS test facility using selected parametric tests performed on the individual wafers. The test results from each wafer are checked for compliance to the specification limits, and the best wafers were then selected for packaging. Although the yield monitors did not form a part of the formal acceptance specifications for wafers, they were used to monitor the quality of the incoming product from different manufacturers. Manufacturers whose products failed to provide satisfactory yields as measured by the yield monitor, were dropped from the list of approved vendors. In addition to the yield monitor, users' test reports are used to assess the quality of a particular fabrication run.

In addition to the process control and yield monitor structures, wafer level reliability test structures developed under a separate DARPA program, were used during the initial vendor qualification programs during the latter part of this contract.

Wafers meeting the electrical inspection criteria were visually inspected before being sent out for sawing and packaging. Commercial assembly houses were used for sawing and assembly into finished parts. All vendors used perform a visual die inspection before assembly and a package inspection after the assembly. To verify these results, MOSIS selected statistical samples from finished lots of parts and performed visual inspection for bond quality, and project identity verification. The sample is selected using the statistical tables provided in MIL STD 105.

4.8 ACCOUNTING PROCEDURES

In order to track customers and costs expended in fabrication runs, a comprehensive computerized accounting system was maintained which functioned in an almost completely automatic mode. The projects submitted were sized by the system upon submission, the areas computed, and the cost of the project was then assessed against the customer's account.

5.0 TECHNOLOGY DESCRIPTIONS

5.1 IC FABRICATION TECHNOLOGIES ACCESSED BY MOSIS

The technologies that were made available through the MOSIS Service during the contract duration ranged from 2μ–0.25μ CMOS to 1.0μ GaAs devices. Even though primarily the type of construction (e.g., CMOS) and minimum feature size may classify a technology, there are a number of other significant features that have to be addressed when making the technology available for wide access. Process differences such as the number of layers of metal and/or polysilicon, or the number and type of wells (in CMOS) can also make a significant difference in the design styles and quality constraints. Most important, perhaps, is which vendors can make the particular technology available for access by the MOSIS Service. The early choice for CMOS technology employed P-Wells on an N-type substrate. This choice was made because with the level of fabrication technology available at the time, the N-type substrate was not inverted as readily as a P-type substrate by the alkali metals, such as sodium, a very common and hard to eliminate contaminant at the time. The inversion of the substrate would result in a shunting path for the current from the well to the edge of the die. As the semiconductor processing techniques improved, eliminating the presence of alkali contaminants from processing areas, processes began to migrate towards the faster N-well technology.

5.1.1 IC TECHNOLOGY DESCRIPTIONS

2μ P-Well CMOS (ANALOG). This technology was fabricated with two levels of polysilicon and two levels of metal. It continues in use. Vendor was Orbit.

2μ N-Well CMOS, (ANALOG) This technology was fabricated with two levels of polysilicon and two levels of metal as well as a limited set of bipolar options. It continues in use. Vendor was Orbit.

1.2μ N-Well CMOS (DIGITAL). Two and three levels of metal and one of polysilicon with a linear capacitor option (for switched capacitor designs). Vendors were Hewlett-Packard.

1.5μ N-Well CMOS. Two levels of metal and polysilicon, NPN transistor options. Vendors: Orbit and AMI.

0.8μ N-Well CMOS (DIGITAL). Two and three levels of metal and one of polysilicon. Vendors were Hewlett-Packard, AMI and IBM.

0.5μ N-Well CMOS (DIGITAL). Three levels of metal and one of polysilicon. Vendors: Hewlett-Packard and AMI.

0.35μ N-Well CMOS (DIGITAL & ANALOG). Five levels of metal, double poly options, linear capacitor options, various process modules. Vendors: CSM, Hewlett-Packard and TSMC.

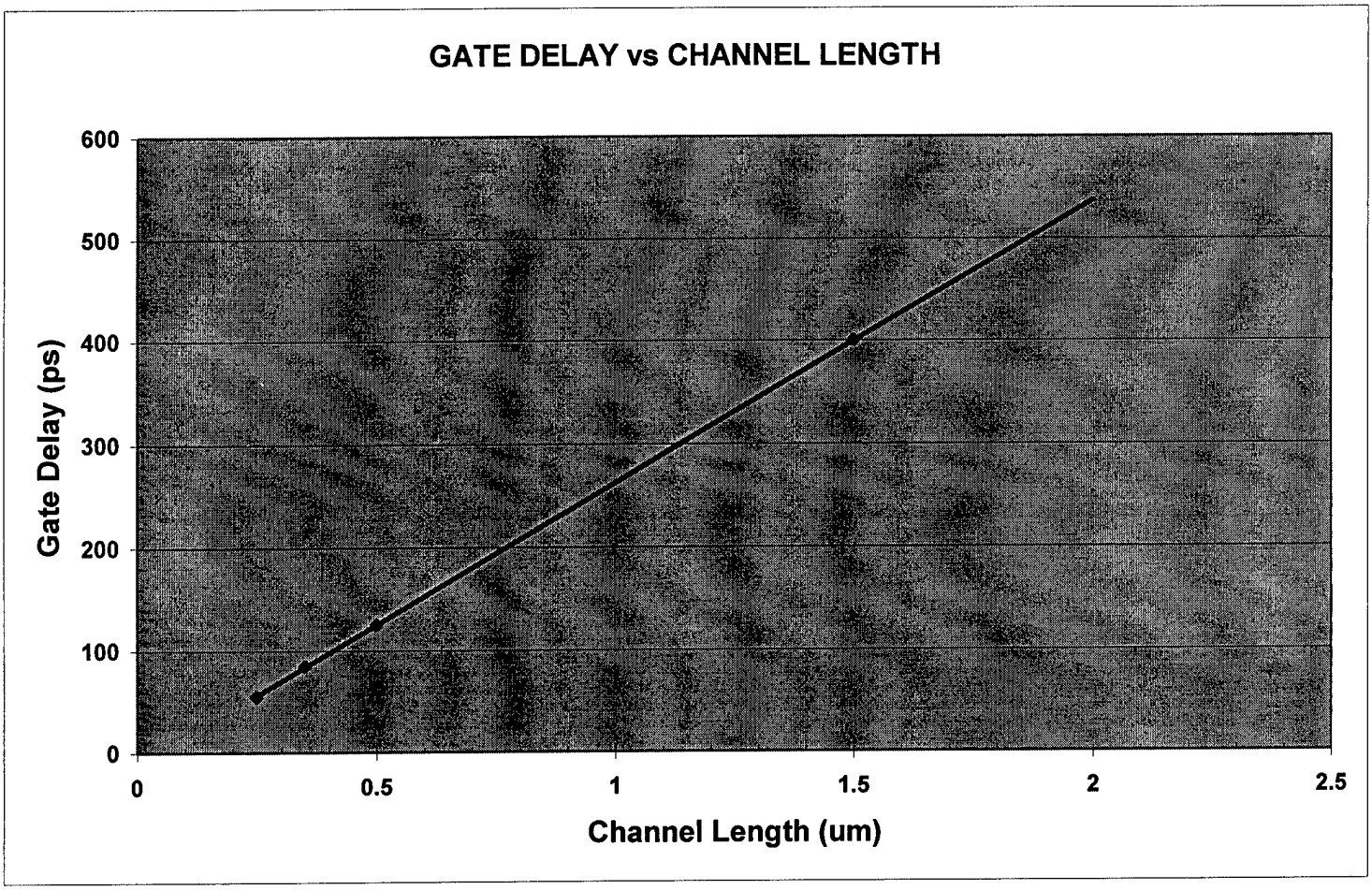
0.25μ N-Well CMOS (DIGITAL). Five levels of metal, double poly options, linear capacitor options, various process modules. Vendors: TSMC.

1.0μ GaAs. DCFL Logic. Vendor Vitesse.

PWB. The MOSIS Service supported a limited PWB brokerage service during the duration of this contract. Design formats were accepted from the users in Gerber format or as film. No board assembly was performed, only bare board fabrication was supported. Primary vendor was Multek.

5.1.1 IC TECHNOLOGY COMPARISONS

The chart below provides a comparison of gate delay in picoseconds (ps) vs. the gate channel length in microns T The difference in delay means that the 0.25um devices are approximately aster than the 2um ones.



5.2 COMPARISON OF PHOTOLITHOGRAPHIC PROCESSES

Advanced IC technologies use photolithographic processes to define the features of the circuits during fabrication. Typically, feature sizes larger than or equal to 2m can use full wafer lithography processes. In these processes, the feature size on the mask is the same size as the feature size on the finished wafer (1X process). Due to the difficulty of maintaining dimensional and alignment control over a wafer of 125-150mm dimension for micron sized features, manufacturers have shifted to stepper based technology for dimensions smaller than 2m. Two types of steppers are in common use: 5X and 1X Ultratech. The 5X steppers find use in all technologies below 2m, whereas the 1X Ultratech steppers find use in the range between 1.2m and 2m. The 1X Ultratech steppers are better suited for prototyping purposes, since the available payload is 900 sqmm (three fields, each one 10x30mm), compared to 200 sqmm (one field, 14x14mm) for the 5X processes. This means that all other things being equal, the cost (not including the masks) for projects should be less by a factor of four when using 1X steppers than 5X. In reality, once the mask costs are taken into account, the price differential is between 2 and 3 times. As dimensions decrease below 1_{μ}, yields and performance favor the 5X process. This is shown in the comparison table below:

Consider a 16M DRAM, with a 0.5m feature size.

CHARACTERISTIC	1X Ultratech	5X Reticle
Min. mask feature size (μ)	0.5	2.5
Registration Accuracy (nm)	16	83
Defect Size Limit (nm)	<70	<350
Surface Flatness (μ)	<0.3	<1.5
Pellicle Particle Limit (nm)	70	350

Since the mask feature sizes are 5x larger for the 5X reticle, the defects that can be tolerated on the mask are also x larger, resulting in a much more tolerant process and higher yields. Unfortunately, the reduction in payload vailable for a prototyping run (where only a small number of parts is desired), results in higher project costs. When ompared with a full wafer lithography run, having a payload of 4500 to 6000 sqmm, the change is even more ramatic.

5.3 YIELD COMPARISONS

5.3.1 YIELD MODELS

During the operation of the MOSIS Service, several yield models were evaluated. The yield models were necessary to provide comparisons between the different manufacturers and to provide data that designers could use to determine if their results were what was expected for the given manufacturer and their chip size. All of the models depend directly on the project area. All other things being equal, the larger the project, the lower the yield for a given process. Three yield models were evaluated and are listed here for reference.

POISSON:
This is the simplest model and assumes a uniform distribution of point defects, i.e., a constant defect density. It tends, however, to underestimate the yield of larger chips. For this reason, this model was discarded early.

$$Y = \exp(-\lambda A)$$

where

Y = yield

A = area of chip

λ = defect density

SEEDS:
Assumes a variable defect density, and in addition, that the probability of having a large defect density is low, and the probability of having a small defect density is high. This model did not provide as good results as Murphy's model and was not used routinely.

$$Y = \exp(-\sqrt{\lambda A})$$

where

Y = yield

λ = defect density

A = Area

MURPHY:

This model assumes a that the defect density is Gaussian, with the lowest value at the center of the wafer. The model showed a good correlation with observed results on both large and small chips. Consequently, it was used consistently for yield estimates.

$$Y = \frac{1 - \exp(-\lambda A)^2}{\lambda A}$$

where

Y = yield

λ = defect density

A = area of chip

6.0 SUMMARY OF RESULTS

6.1 ACCESS TO ADVANCED TECHNOLOGIES

(1) Provided access to advanced 2_{μ}, 1.2_{μ}, 0.8_{μ}, 0.5_{μ}, 0.35_{μ} and, 0.25_{μ} CMOS technology and MultiChip Module (MCM) as they became commercially available to the prototyping service. A total of 9,351 IC designs were processed by the MOSIS Service in 371 different fabrication runs.

(2) Qualified a 0.35_{μ} CMOS Bulk digital process from Hewlett Packard as well as 0.35_{μ} and 0.25_{μ} processes from TSMC. These provided slightly more than a 50% increase in speed over the previous 0.5_{μ} digital process. Our standard 31-stage ring oscillator operates at 190 MHz in this technology, compared to 120Mhz in the 1_{μ} technology.

(3) Qualified and provided access to a 1.0 $_{\mu}$ VLSI DCFL GaAs process.

(4) Qualified and provided access to a 1.5_{μ} Analog/Digital process from Orbit and AMI.

(5) Generated and distributed several sets of CMOS scaleable design rules for use by the design community.

(6) Generated and distributed sets of I/O pads for use by the design community.

6.2 TECHNOLOGY TRANSFER

During the duration of this contract, USC/ISI provided support for the IC prototyping run closing system (developed initially for use by the MOSIS Service) and ported to the DoD for internal use during a prior contract. USC/ISI also provided support for the transferred technology.

7.0 SUMMARY OF MOSIS SERVICE FABRICATION RUNS

Four principal products resulted from this activity. The first was the access to the U.S. semiconductor industry for chips, packages, testing, printed circuit boards, and advanced packaging provided to the DARPA research community. The second was the methodology of procuring small volume prototype parts in an economical fashion. A third product was the access provided to Universities and other NSF sponsored institutions to a low cost prototyping service. The fourth product was the transfer of the run-closing technology developed under this program to the Department of Defense, for use in their own classified work.

During the five years covered by this report, the MOSIS Service of USC/ISI processed a total of 9,351 projects through 371 fabrication runs in different technologies, ranging from 2_{μ} CMOS to 1.0 μ GaAs. These projects came from (1) DARPA sponsored research organizations, (2) university class projects from the DARPA/NSF sponsored university VLSI classes, (3) other Government organizations and (4). DoD contractors and (5) industrail firms.

The table in the following two pages summarizes the prototype fabrication volume through the MOSIS Service for the five years of the contract duration. The two columns labeled "GOV" and "NON-GOV" list the number of projects submitted either under direct government sponsorship (groups 1-3 above) and the total of groups 3 and 4 respectively.

TECHNOLOGY	YEAR	# RUNS	NON-GOV	GOV	TOTAL	Ave./Run
Jun95-Jun96	UFY96					
MCM_D		6	7	5	12	2
SCN05		11	60	35	95	8.6
SCN08		20	208	53	261	13.1
SCN12		17	210	75	285	16.8
SCN15		1	37	0	37	37
SCNA20		8	413	856	1269	158.6
VITESSE_HGAAS3		3	27	4	31	10.3
TOTALS		66	962	1028	1990	30.2
Jul96-Jun97	UFY97					
MCM_D		2	4	6	10	5
SCN05		21	222	78	300	14.3
SCN08H		18	183	41	224	12.4
SCN12		19	167	92	259	13.6
SCN15		1	48	35	83	83
SCNA20		8	393	985	1378	172.3
VITESSE_HGAAS3		3	25	0	25	8.3
TOTALS		72	1042	1237	2279	31.7

TECHNOLOGY	YEAR	# RUNS	NON-GOV	GOV	TOTAL	Ave./Run
Jul97-Jun98	**UFY98**					
MCM_D		3	1	2	3	1
SCN035		4	75	8	83	20.8
SCN05		33	300	46	346	10.5
SCN08		24	137	4	141	5.9
SCN15		22	307	322	629	28.6
SCNA20		4	218	444	662	165.5
SIGE		1	9	1	10	10
VITESSE_HGAAS3		1	6	1	7	7
TOTALS		**92**	**1053**	**828**	**1881**	**20.4**
Jul98-Jun99	**UFY99**					
SCN025		1	13	0	13	13
SCN035		13	228	2	230	17.7
SCN05		32	334	76	410	12.8
SCN08H		10	69	0	69	6.9
SCN15		9	319	301	620	68.9
SCNA20		4	153	233	386	96.5
SIGE		1	10	13	23	23
SOI05		1	24	0	24	24
VITESSE_HGAAS4		1	7	1	8	8
TOTALS		**72**	**1157**	**626**	**1783**	**24.8**
Jul99-Jun00	**UFY00**					
SCN025		12	85	0	85	7.1
SCN035		17	208	1	209	12.3
SCN05		26	246	124	370	14.2
SCN10		1	4	0	4	4
SCN15		15	315	330	645	43
SCNA20		2	44	49	93	46.5
SOI05		2	12	0	12	6
TOTALS		**75**	**914**	**504**	**1418**	**18.9**